REMARKS

In the Office Action, the Examiner rejected claim 21 under 35 USC § 112 and claims 1, 4-6, 9-12-18 and 21-24 under 35 USC § 103. These rejections are fully traversed below.

Claims 1, 5 and 21 have been amended. Thus, claims 1, 4-6, 9-20 and 21-24 are pending in the application. Reconsideration of the application is respectfully requested based on the following remarks.

REQUEST FOR WITHDRAWAL OF FINALITY OF OUTSTANDING OFFICE ACTION

The finality in the above referenced office action is believed to be premature and therefore reconsideration is respectfully requested. The finality is believed to be premature since the amendment to claim 5 did not necessitate a new ground(s) of rejection. Claim 5 was amended to include the limitations from dependent claims 7 and 8. No other limitations were added to claim 5. See for example, the REMARKS section of the previous amendment A where it states the above amendment. Claims 5, 7 and 8 were rejected in the first Office Action via 102 rejections including Prall and La. Both of these rejection were removed in the subsequent Office Action. Claim 5, which includes the limitations from claims 7 and 8, was rejected in the second Office Action via 103 rejections that included combination of La with Guo and La with Loan. Neither Guo nor Loan had been used to reject these limitations in the previous Office Action. Accordingly, the finality of the outstanding Office Action should be withdrawn.

ISSUES UNDER 35 USC 112(2)

Claim 21 has been rejected under 35 USC 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is believed that the rejection is overcome by the amendment made above, i.e., the term "such as" was removed from claim 21 and the term "processing task" was changed to --etching task--.

ISSUES UNDER 35 USC 103(a)

Claims 1, 4-6, 9-12, 14-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *La* et al. (U.S. Patent No. 6,136,510) in view of *Guo* et al. (U.S. Patent No. 6,251,759).

While *La* may disclose scrubbing and etching steps and *Guo* may disclose process chambers and preclean chambers, neither reference teaches or suggests "etching the process side of the wafer...without performing any intervening processing steps between etching and removal steps," as required by claim 1, "...etching the process side of the wafer in the processing module without performing any intervening processing steps between the steps of cleaning the backside of the wafer and etching the process side of the wafer..." as required by claim 5.

Gou is completely silent to etching, i.e., the process chambers are for depositing copper using metallization or sputtering techniques, and cleaning the backside of a wafer, i.e., only discusses preclean chambers. And while *La* may disclose scrubbing and an etching step, *La* also discloses performing an **intervening** photolithographic technique between the scrubbing and etching steps. Scrubbing does **not** occur between the photolithographic technique and the etching step. In fact, because of this one may argue that *La* teaches away from the above mentioned limitations. *La* repeatedly states, double sided scrubbing is conducted preferably immediately prior to forming a photomask, to remove particulate contaminants from the backside of the wafer thereby significantly improving the accuracy of the photolithographic technique employing the photomask (see for example Col. 4, lines 25-29, Col. 4, lines 43-48). As should be appreciated, *La* addresses the problem of photolithographic failure and thus scrubbing occurs prior to the photolithographic technique not prior to an etching technique as required by claim 1.

In the embodiments where *La* includes etching steps, *La* states, "a conductive pattern is formed on the dielectric layer and a second dielectric layer is deposited on the conductive pattern. Double-sided wafer scrubbing is performed, preferably immediately subsequent to depositing the second dielectric layer and/or immediately before forming a photoresist mask on the second dielectric layer. The photoresist mask is typically formed by depositing a layer of photoresist material and performing any of various conventional photolithographic techniques. The second dielectric layer is then etched through the photoresist mask to form a through

hole...(Col. 5, lines 16-25)," and "a dielectric layer is deposited on the frontside of a semiconductor wafer and double sided scrubbing is performed, preferably immediately thereafter. A photoresist material is then deposited on the dielectric layer, preferably immediately after double sided wafer scrubbing and a photoresist mask is formed defining a conductive pattern...The underlying dielectric layer is then etched through the photoresist mask to form a plurality of trenches...(Col. 5, lines 32-45)." Again, *La* teaches performing intervening processing steps (e.g., photolithographic technique) between the etching and scrubbing steps. This goes against the limitation of claim 1 described above. Accordingly, the rejection is unsupported by the art and should be withdrawn.

Also in contrast to *La* and *Guo*, claim 5 specifically requires, "...wherein only the backside of the wafer is cleaned in the cleaning module so as not to damage the process side of the wafer..." *Guo* is silent to cleaning the backside of the wafer. And while *La* may disclose scrubbing the backside of the wafer, *La* does not teach or suggest scrubbing only the backside of the wafer. In *La*, both sides of the wafer are scrubbed. *La* repeatedly states that his invention comprises a less severe and more cost effective solution for reducing photolithographic failures by performing a double-sided scrubbing operation using conventional in place equipment. For example, *La* states, "The present invention addresses and solves the problem in a cost effective and efficient manner, preferably by utilizing existing production equipment. The solution ...resides in scrubbing the backside of the wafer preferably by performing a double sided scrubbing operation at strategic times...(Col. 3. lines 41-48)." See also Col. 3, lines 59-62, where *La* teaches away from CMP of the wafer backside by expressly stating that a double sided scrubbing operation is performed.

The Examiner asserted that *La* teaches "only backside scrubbing" in Col. 4 lines 1-6. The Applicant respectfully disagrees. La is simply further describing the backside scrubbing operation of a double sided scrubbing operation. This can be seen in the way the section is written. First, *La* states, "The present invention comprises a less severe and more cost effective solution...by performing a double sided scrubbing operation...Col. 3, lines 59-62.". Immediately thereafter in Col. 4 lines 1-6, *La* states that "...backside scrubbing is effected by processing only the backside of the wafer by a scrubbing operation..." This language implies that backside scrubbing, not scrubbing in general, is only performed on the backside of the wafer. That is, backside scrubbing is defined by scrubbing only the backside of the wafer. This phrase does not exclude front side scrubbing from the overall scrubbing operation as is required

by claims 5 (it only further defines what is meant by backside scrubbing). Taken in context with the aim of the invention in *La* (e.g., double sided scrubbing), one would simply not think that this is precluding front side scrubbing. If *La* was in fact describing a different embodiment (e.g., other than double sided scrubbing), then "backside scrubbing" should have been replaced with "scrubbing."

The Examiner also asserted that *La* exemplifies the embodiment of exclusive backside cleaning in his own Patent 5,780,204. This, however, is incorrect in that 5,780,204 describes reducing photolithographic failures by chemical-mechanical planarization or polishing (CMP) a wafer backside. CMP is not cleaning. In fact, La states, "double sided scrubbing is typically conducted subsequent to performing post metal deposition CMP to remove contaminants generated during CMP (Col. 4, lines 21-24). As should be appreciated, the purpose of cleaning is to remove particles not generate them as in CMP. Accordingly, the rejection is unsupported by the art and should be withdrawn.

Although the rejections to the dependent claims 4, 6, 9-12, 14-18 should be withdrawn for at least the reasons as above, it should be noted that they offer additional language that is unsupported by the art.

Claims 1, 4-6, 9-11, 13 and 14-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *La* et al. (U.S. Patent No. 6,136,510) in view of *Loan* et al. (U.S. Patent No. 6,136,725).

Loan does not overcome the deficiencies of *La*. That is, neither reference teaches or suggests, "etching the process side of the wafer...without performing any intervening processing steps between etching and removal steps," as required by claim 1, "...etching the process side of the wafer in the processing module without performing any intervening processing steps between the steps of cleaning the backside of the wafer and etching the process side of the wafer..." as required by claim 5, and further, "...wherein only the backside of the wafer is cleaned in the cleaning module so as not to damage the process side of the wafer..." as required by claim 5. With regards to *La*, see arguments made above. With regards to *Loan*, *Loan* is directed at deposition rather than etching and further does not teach or suggest sequential cleaning steps associated with a wafer. Accordingly, the rejection is unsupported by the art and should be withdrawn.

Although the rejections to the dependent claims 4, 6, 9-11, 13-18 should be withdrawn for at least the reasons as above, it should be noted that they offer additional language that is unsupported by the art.

Claim 21-24 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *La* in view of *Hiatt* (U.S. 5,966,635) and in further view of *Fukasawa (U.S. 5 310,453).*

The rejection should be withdrawn for at least the reasons given above (e.g., claim 21 has similar limitation to claims 1 and 5). That is, none of the references teach or suggest "providing a cleaning module for cleaning the backside of the wafer and a plasma reactor for performing an etching task...removing the wafer from the cleaning module and thereafter introducing the wafer into the process chamber of the plasma reactor without performing any intervening processing steps therebetween..." or "...wherein only the backside is cleaned so as not to damage the process side of the wafer..." as required by claim 21. See argument above with regards to *La*. *Hiatt* and *Fukasawa* do not overcome the deficiencies of *La*. *Hiatt* and *Fukasawa* fail to disclose removing residual material from a wafer. The most that can be said is that *Hiatt* discloses applying a solvent to the surface of a chuck to remove residual material that adheres to the surface of the chuck. Accordingly, the rejection is unsupported by the art and should be withdrawn.

Although the rejections to the dependent claims 22-24 should be withdrawn for at least the reasons as above, it should be noted that they offer additional language that is unsupported by the art.

SUMMARY

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Quin C. Hoellwarth
Reg. No. 45, 738

P.O. Box 778
Berkeley, CA 94704-0778
(650) 961-8300

APPENDIX

1. (Twice Amended) A method of processing a wafer having a process side and a back side, comprising:

removing un-wanted particles from the back side of the wafer in order to maintain the desired relationship between the backside of the wafer and a chucking surface;

placing the wafer on a chucking surface after removing the unwanted particles from the back side of the wafer;

[performing a specific processing task on] **etching** the process side of the wafer **[for the first time]** after placing the wafer on the chucking surface **and without performing any intervening processing steps between the etching and removal steps**.

5. (Twice Amended) A method of processing a wafer having a process side and a backside opposite the process side, the method comprising:

providing a semi-dry cleaning module for cleaning the backside of the wafer and a processing module for performing a processing task on the process side of the wafer;

receiving the wafer for processing;

loading the wafer into the cleaning module;

cleaning the backside of the wafer in the semi-dry cleaning module to remove particles therefrom, wherein only the backside of the wafer is cleaned in the semi dry cleaning module so as not to damage the process side of the wafer;

transferring the wafer to the processing module;

loading the wafer into the processing module; and

[performing the processing task on] **etching** the process side of the wafer in the processing module **without performing any intervening processing steps between the steps of cleaning the backside of the wafer and etching the process side of the wafer**.

21. (Once Amended) A method of processing a wafer having a process side and a backside opposite the process side, the method comprising:

providing a cleaning module for cleaning the backside of the wafer and a plasma reactor for performing a**n etching** **[processing]** task **[such as etching or deposition]** on the process side of the wafer, the plasma reactor having a process chamber within which a plasma is formed for

the processing task and a chuck for supporting the wafer during the processing task, the chuck being disposed inside the process chamber, the chuck including a heat transfer system;

cleaning the backside of the wafer in the cleaning module to remove particles therefrom, wherein only the backside is cleaned so as not to damage the process side of the wafer;

removing the wafer from the cleaning module and thereafter introducing the wafer into the process chamber of the plasma reactor **without performing any intervening processing steps therebetween**;

placing the wafer on the chuck; and

holding the backside of the wafer relative to a top surface of the chuck with an electrostatic force, the cleaned backside of the wafer preventing undesirable gaps from forming between the backside of the wafer and the top surface of the chuck;

performing the **[processing] etching** task with the plasma on the process side of the wafer in the process chamber of the plasma reactor; and

distributing a heat transfer gas to the backside of the wafer via the heat transfer system during the **[processing] etching** task, the cleaned backside of the wafer reducing heat transfer gas faults caused by undesirable gaps.